LISTING OF THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Previously Presented) A DC-DC converter comprising:

a synchronous semiconductor device; and

a control semiconductor device;

wherein at least one of said semiconductor devices includes:

a semiconductor body of a first conductivity which includes a channel region of a second conductivity and a major surface;

an active region formed in said semiconductor body, said active region including a plurality of spaced trenches each less than 0.5 microns wide and each extending through said channel region;

a gate structure disposed in each said trench, each gate structure including a gate oxide layer disposed at least on sidewalls of a trench and a gate electrode disposed adjacent said gate oxide layer;

conductive regions of said first conductivity formed in said channel region adjacent each said trench;

highly doped contact regions of said second conductivity formed in said channel region each being laterally confined between two opposing conductive regions;

a metallic contact in contact with said conductive regions and said highly doped contact regions; and

a termination structure, said termination structure including,

a termination trench having a slanted sidewall formed in said semiconductor body, and a grown field oxide layer formed in said termination trench below said major surface, a polysilicon field plate formed over said field oxide layer, and a low temperature oxide body over said polysilicon field plate, wherein said field oxide layer is thicker than said gate oxide layer, wherein said metallic contact extends over said low temperature oxide body, and wherein said semiconductor body of said first conductivity extends from said trench to the bottom of said termination trench.

Claims 2-3 (canceled).

4. (Previously Presented) A semiconductor device according to claim 1, wherein said trench includes an oxide mass formed at its bottom, said oxide mass being thicker than said gate oxide layer.

5. (Previously Presented) A semiconductor device according to claim 4, further comprising a semiconductor substrate of said first conductivity, said semiconductor body being formed over said semiconductor substrate, wherein said conductive regions are electrically connectable to said semiconductor substrate through invertible channels adjacent said trench.

6. (Original) A semiconductor device according to claim 5, wherein said conductive regions are source regions.

7. (Previously Presented) A semiconductor device according to claim 1, wherein the depth of said trench has been selected to achieve an optimum figure of merit.

8. (Previously Presented) A semiconductor device according to claim 1, wherein said trench is a stripe.

9. (Previously Presented) A semiconductor device according to claim 1, wherein said trench is a cell.

10. (Original) A semiconductor device according to claim 9, wherein said cell is hexagonal.